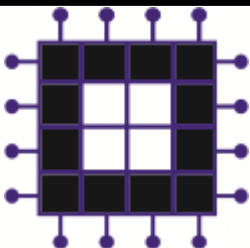


Summer Training
(Four/Six/Eight Weeks)
in
VLSI Design
(RTL using Verilog & FPGA)

***An initiative by Industry Experts
from Cadence, Atrenta & Patni
with qualification from
IITs and BITS-Pilani***

***Training Partners of Cadence Design
Systems and Mentor Graphics
(Worldwide EDA Giants)***



DKOP Labs Pvt. Ltd.

Knowledge, Operations and Practices

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Tel: 0120-4274237; Mob: +91-9971792797, +91-9910101496, +91-9780280410
Email: info@dkoplabs.com; Web: <http://www.dkoplabs.com>

MODULE TOPICS

MODULE 1: VLSI DESIGN FLOW

MODULE 2: DIGITAL ELECTRONICS REFRESHER

MODULE 3: VERILOG HDL

1. Hierarchical Modeling Concepts
2. Basic Concepts
3. Modules and Ports
4. Gate-Level Modeling
5. Dataflow Modeling
6. Behavioral Modeling
7. Useful Modeling Techniques

MODULE 4: BASICS OF TESTBENCHES

1. Design Testing Concepts
2. Test Bench Generation
3. Simulation & Verification using Test Benches

MODULE 5: MINI PROJECT IN VERILOG

1. Project Study
2. Design & Implementation using Mentor Graphics ModelSim simulation tools
3. Presentation
4. Document submission
5. Evaluation of Project

MODULE 6: FPGA BASICS

1. FPGA Kit Introduction
2. Block RAM
3. FPGA Kit interfacing and configuration
 - a. Switch Interfacing
 - i. Combinational
 - ii. Sequential
 - b. Seven Segment Display

MODULE 7: FPGA ADVANCED

1. **FPGA Kit interfacing and configuration – Advanced**
 - a. **PS2 Mouse/Keyboard**
 - b. **VGA Controller**
2. **ChipScope Pro Analyzer**
3. **Configuring & Utilizing FPGA Resources**
 - a. **Global Clock Resources**
 - b. **Internal Description of LUT**
 - c. **Dedicated Arithmetic functions-Adder & Multipliers**
 - d. **Macro functions**
4. **Hardware Implementation of Verilog Project**

MODULE 8: LINUX OPERATING SYSTEM & SHELL SCRIPTING

1. **Introduction to Linux OS**
2. **Commands for Managing files and directories**
3. **Methods of Securing Files in Linux**
4. **Document Processing commands**
 - a. **Filters**
 - b. **Redirection**
 - c. **Pipes**
 - d. **Wildcards**
5. **Creating files using the vi editor**
6. **vi Commands**
7. **Automating tasks using shell scripts**
8. **Using conditional execution in shell scripts**
 - a. **Arithmetic Conditions**
 - b. **String Conditions**
 - c. **File/Directory conditions**
9. **Managing repetitive tasks using shell scripts**
 - a. **Loops – While, Until, for**
 - b. **break and continue**
10. **Parameters Handling**

MODULE 9: SOFT SKILLS

1. **Resume Writing**
2. **Interview Facing Skills**

Four weeks training will cover modules 1, 2, 3, 4, 5 & 9

Six Weeks training will cover modules 1, 2, 3, 4, 5, 6 & 9

Eight Weeks training will cover modules 1, 2, 3, 4, 5, 6, 7, 8 & 9

PROGRAM DETAILS

Duration : Four/Six/Eight Weeks
(5 days/week, Mon-Fri, 4 hours/day)

Fee Details

Four Weeks : Rs 8,000/- per student plus GST @ 18%

Six Weeks : Rs 12,000/- per student plus GST @ 18%

Eight Weeks : Rs 16,000/- per student plus GST @ 18%

Payment Schedule

- Rs 1,180/- (1000 + GST @ 18%) at the time of Registration
- Balance amount on the day of joining

TOOLS

Our labs are equipped with State-of-the-art *Licensed EDA Tools* from **Mentor Graphics**

BENEFITS FOR THE STUDENTS

- Helps you in understanding the **practical** and **industrial applications** of academic curriculum
- Build your knowledge to develop **innovative projects** during your final year of engineering
- Enhances the Skill-Set in your resume for **better placement prospects** within the **semiconductor industry**
- Helps the aspirants of **higher studies abroad** to face the stiff competition from students of other countries
- Build your confidence through **hands on exposure** to various **tools & technologies**

TEAM OF TRAINERS

DKOP Labs is proud to have highly qualified and experienced professionals from Industry, Research and Academics. For details, [click here](#).

PLACEMENTS

We have been providing excellent placement platform to our trainees in companies like **Cadence, Xilinx, ST Microelectronics, Samsung, Synopsys, Mentor Graphics, CMC Limited, SmartPlay, TrueChip, Agnisys, DKOP Labs, etc.** For detailed list, [click here](#).

DKOP PARTNERSHIPS

TRAINING PARTNER OF ESSCI – NSDC (ELECTRONICS SECTOR SKILL COUNCIL OF INDIA – NATIONAL SKILL DEVELOPMENT CORPORATION)

TECHNOLOGY PARTNER OF CADENCE DESIGN SYSTEMS

QUESTA VANGUARD PARTNER OF MENTOR GRAPHICS

HEP PARTNER OF MENTOR GRAPHICS

ON-CAMPUS PROGRAMS

We have conducted on-campus training programs at following colleges:

1. PTU Nalanda Campus, Mohali
2. NIT, Jalandhar
3. Lovely Professional University, Phagwara
4. Maharaja Surajmal Institute of Technology, Delhi
5. Sharda Group of Institutions, Agra
6. Sharda University, Greater Noida
7. Thapar University, Patiala
8. Galgotia College of Engineering & Technology, Greater Noida
9. MGM College of Engineering & Technology, Noida

10. Manipal University, Jaipur
11. Greater Noida Institute of Technology, Greater Noida
12. St Margaret College of Engineering & Technology, Neemrana
13. Echelon Institute of Technology, Faridabad
14. Maharaja Agarsen College, Delhi University
15. UIET, Kurukshetra University
16. RIMT, Mandi Gobindgarh, Punjab

and many more...